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Design Of Reversible Fault Tolerent Decoder Using MOS Transistors

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Abstract—This paper demonstrates the reversible logic synthesis for the n-to-2n decoder, where n is the fault tolerant Fredkin and Feynman double gates. Thus, the entire scheme inherently becomes fault tolerant. Algorithm for designing the generalized decoder has been presented. In addition, several lower bounds on the number of constant inputs, garbage outputs and quantum cost of the reversible fault tolerant decoder have been proposed.Transistor simulation of the proposed design are shown in microwind 3.0 version where power area and delay are calculated.

***Index Terms*—Decoder, Delay, Garbage Output, Low Power Design, Quantum Cost, Reversible & Fault Tolerant Computing.**

1. INTRODUCTION

Reversible Logic has gained importance in the recent past. The rapid decrease in the size of the chips has lead to the exponential increase in the transistor count per unit area. As a result, the energy dissipation is becoming a major barrier in the evolving nano-computing era. Reversible logic ensures low energy dissipation R.W. Keyes et.al (1970), C.H. Bennet (1988). An operation is said to be physically reversible if there is no energy to heat conversion and no change in entropy. In reversible logic, the state of the computational device just prior to an operation is uniquely determined by its state just after the operation. In other words, no information about the computational state can ever be lost.

Hence the reversible logic can be viewed as a deterministic state machine. R.Landauer (1961) has shown that for every bit of information that is erased during an irreversible logic computation kTln2 joules of heat energy is generated, where k is the Boltzmann constant and T is the temperature in Kelvin at which the system is operating. C.H.Bennett (1973) showed that the kTln2 amount of energy dissipation would not occur if a computation is carried out in a reversible way.

Computations performed by the current computers are commonly irreversible, even though the physical devices that execute them are fundamentally reversible. At the basic level, however, matter is governed by classical mechanics and quantum mechanics, which are reversible. With computational device technology rapidly approaching the elementary particle level, it has been argued many times that this effect gains in significance to the extent that efficient operation of future computers requires them to be reversible C.H.Bennett (1988), R.Landauer (1961). Hence, reversible logic is gaining grounds.

A reversible gate is a logical cell that has the same number of inputs and outputs. Also, the input and output vectors have a one-to-one mapping. Direct fan-outs from the reversible gate are not permitted. Feedbacks from gate outputs to inputs are not allowed. A reversible gate with n-inputs and n-outputs is called a n x n reversible gate. Several reversible gates have been designed till date that is discussed below. The Feynman gate R.Feynman (1985) shown in Figure 1 is one of the popular example of a 2 x 2 reversible gate. In this gate the first input is passed to the output without any change and the second output is the XOR of the first and second inputs. Toffoli Gate T.Toffoli (1980) is a n x n universal reversible gate. The first n - 1 input are directly passed to the corresponding outputs and the nth output is the logical XOR of the nth input with the logical AND of all first n – 1 inputs. The 3 x 3 Toffoli gate is shown in Figure 2. E.Fredkin (1982) proposed a 3 x 3 universal reversible gate. The Fredkin gate functions as a multiplexer with the select signal as the first input. Functionality of the Fredkin gate is shown in Figure 3. Many other gates have been proposed that include Kerntopf gate by P.Kerntopf (2002) and Margolus gate by N.Margolus (1988). An elaborate list of reversible gates studied in the literature is presented in P.Kerntopf (2002).

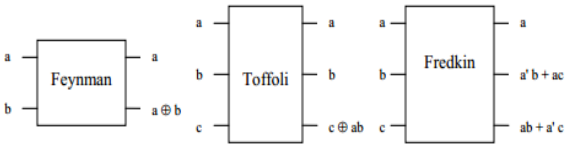


Fig.1. Feynman Gate Fig.2. 3x3 Toffoli Gate Fig.3. Fredkin Gate

2. PREVIOUS METHOD

The most recently reported work D.P.Vasudevan et.al (2004) focuses on the implementations using particular reversible gates. The technique proposed in this paper can be employed to convert any reversible circuit with arbitrary number of gates to an online testable reversible one and is independent of the type of reversible gate used. The constructed circuit can detect any single bit errors that include single bit stuck-at-fault and single event upset S.Karp et.al (1993). An important advantage of the technique is that the logic design of a reversible circuit remains the same and the reversible circuit need not be redesigned for adding the testability feature to it. Another advantage is that the technique ensures that the garbage generated during the process of conversion to testable reversible circuit is minimized. The proposed technique is illustrated using an example that converts a decoder circuit that is designed by reversible gates to an online testable reversible decoder circuit.

A. Testing Reversible Circuits

An *n*×*n reversible gate* is a data stripe block that uniquely maps between input vector *Iv* = (*I*0, *I*1, ..., *In*−1) and output vector *Ov* = (*O*0,*O*1, . . . , *On*−1) denoted as *Iv* ↔ *Ov*. Two prime requirements for the reversible logic circuit are as follows [14]:

- There should be equal number of inputs and outputs.
- There should be one-to-one correspondence between inputs and outputs for all possible input-output sequences.

A *Fault tolerant gate* is a reversible gate that constantly preserves same parity between input and output vectors. More specifically, an $n \times n$ fault tolerant gate clarifies the following property between the input and output vectors [12]:

$$I_0 \oplus I_1 \oplus \ldots \oplus I_{n-1} = O_0 \oplus O_1 \oplus \ldots \oplus O_{n-1} \qquad (1)$$

Parity preserving property of Eq.1 allows detecting a faulty signal from the circuit's primary output. Researchers [11],[12], [15] have showed that the circuit consist of only reversible fault tolerant gates preserves parity and thus able to detect the faulty signal at its primary output.

B. Qubit And Quantum Cost

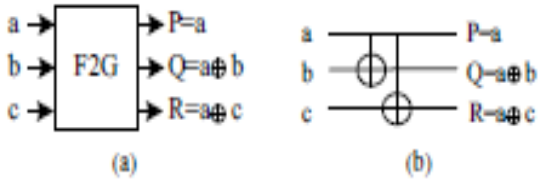
The main difference between the *qubits* and conventional bits is that, qubits can form linear combination of states |0> or |1> called superposition, while the basic states |0> or |1> are an orthogonal basis of two-dimensional complex vector [3]. A superposition can be denoted as, $|\psi> = \alpha|0> + \beta|1>$, which means the probability of particle being measured in states 0 is $|\alpha|2$, or results 1 with probability $|\beta|2$, and of course $|\alpha|2 + |\beta|2 = 1$ [16]. Thus, information stored by a qubit are different when given different α and β. Because of such properties, qubits can perform certain calculations exponentially faster than conventional bits. This is one of the main motivations behind the quantum computing. The *quantum cost* for all 1×1 and 2×2 reversible gates are unity.Hence, quantum cost of a reversible gate or circuit is the total number of 2×2 quantum gate used in that reversible gate or circuit.

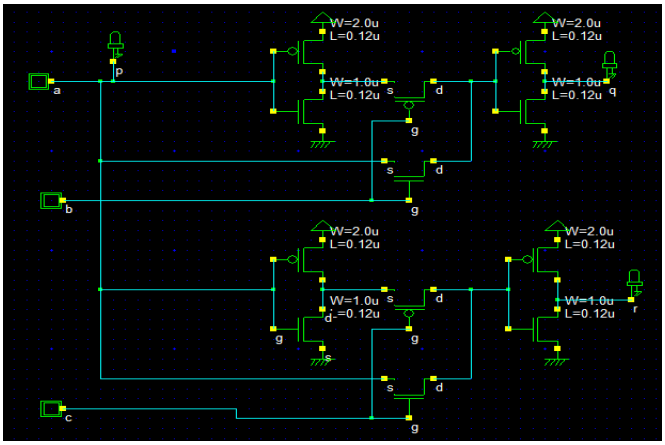
C. Delay, Garbage Output And Hardware Complexity

The *delay* of a circuit is the delay of the critical path. The path with maximum number of gates from any input to any output is the critical path [1]. There may be more than one critical path in a circuit and it is an NP-complete problem to find all the critical paths [17]. So, researchers pick the path which is the most likely candidates for the critical paths [18]. Unused output of a reversible gate (or circuit) is known as *garbage output*, *i.e.*, the output which are needed only to maintain the reversibility are the garbage output. The number of basic operations (Ex-OR, AND, NOT etc.) needed to realize the circuit is referred to as the *hardware complexity* of the circuit. Actually, a constant complexity is assumed for each basic operation of the circuit, such as, α for Ex-OR, β for AND, γ for NOT etc. Then, total number of operations are calculated in terms of α, β, and γ.

D. Popular Reversible Fault Tolerant Gates

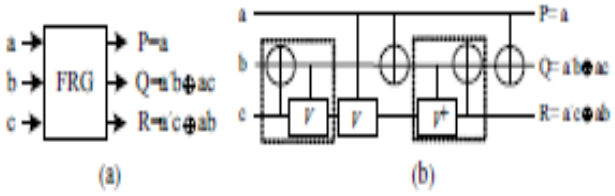
1) Feynman Double Gate: Input vector (*Iv*) and output vector (*Ov*) for 3 × 3 reversible Feynman double gate (*F*2*G*) is defined as follows [19]: *Iv* = (*a, b, c*) and *Ov* = (*a, a* ⊕ *b, a* ⊕ *c*). Block diagram of *F*2*G* is shown in Fig. 1(a). Fig. 1(b) represent the quantum equivalent realization of *F*2*G*. From Fig. 1(b) we find that it is realized with two 2×2 Ex-OR gate, thus its quantum cost is two (Sec. II-B). According to our design procedure, twelve transistors are required to realize *F*2*G* reversibly as shown in Fig. 1(c). Fig. 3(a) represents the corresponding timing diagram of *F*2*G*.

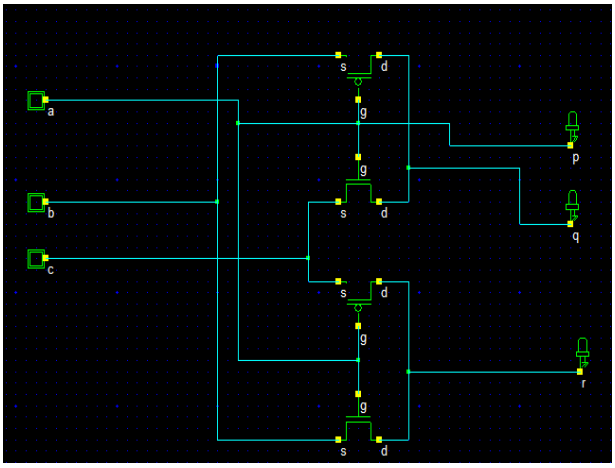




(C) Transistor Realization of Feynamn double gate

***2)* Fredkin Gate:** The input and output vectors for 3 × 3 Fredkin gate (*FRG*) are defined as follows [20]: *Iv* = (*a, b, c*) and *Ov* = (*a, a_b* ⊕ *ac, a_c* ⊕ *ab*). Block diagram of *FRG* is shown in Fig. 2(a). Fig. 2(b) represents the quantum realization of *FRG*. In Fig. 2(b), each rectangle is equivalent to 2 × 2 quantum primitives, therefore its quantum cost is considered as one [13]. Thus total quantum cost of *FRG* is five. To realize the *FRG*, four transistors are needed as shown in Fig. 2(c) and its corresponding timing diagram is shown in Fig. 3(b).





(c) Transistor Realization of Fredkin gate

3. PROPOSED METHOD

A. DECODER

Decoders are the collection of logic gates fixed up in a specific way such that, for an input combination, all outputs *terms* are low except one. These *terms* are the *minterms*. Thus, when an input combination changes, two outputs will change. Let, there are *n* inputs, so number of outputs will be 2*n*. There are several designs of reversible decoders in the literature. To the best of out knowledge, the designs from [7] are the only reversible design that preserves parity too.

B. PROPOSED REVERSIBLE FAULT TOLERANT DECODER

Considering the simplest case, *n*=1, we have a 1-to-2 decoder. Only a *F*2*G* can work as 1-to-2 Reversible Fault tolerant Decoder (RFD) as shown in Fig. 4(a) and its corresponding timing diagram is shown in Fig. 4(b). From now on, we denote a reversible fault tolerant decoder as RFD.

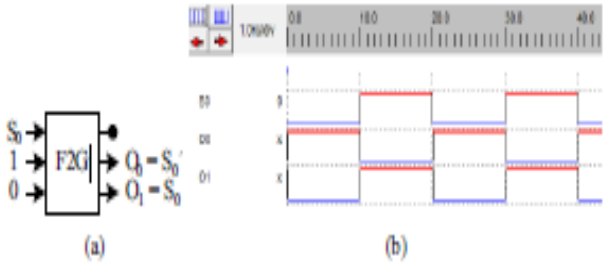


Fig. 5(a) and Fig. 5(d) represent the architecture of 2-to-4 and 3-to-8 RFD, respectively. Timing diagram of Fig. 5(a) is shown in Fig. 5(c). From Fig. 5(d), we find that 3-to-8 RFD is designed using 2-to-4 RFD, thus a schema of Fig. 5(a) is created which is shown in Fig. 5(b). Algorithm 1 presents the design procedure of the proposed *n*-to-2*n* RFD. Primary input to the algorithm is *n* control bits. Line 6 of the proposed algorithm assigns the input to the Feynman double gate for the first control bit (*S*0), whereas line 9 assigns first two inputs to the Fredkin gates for all the remaining control bits. Line 10-12 assign third input to the Fredkin gate for *n* = 2.

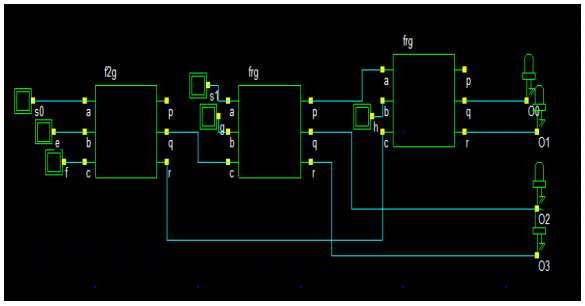


Fig 5(a): Block diagram of the proposed 2-to 4 RFD

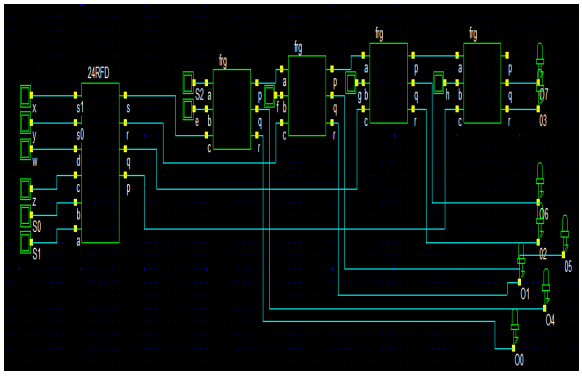
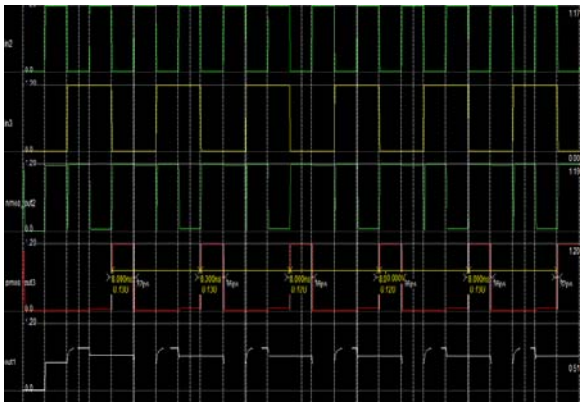
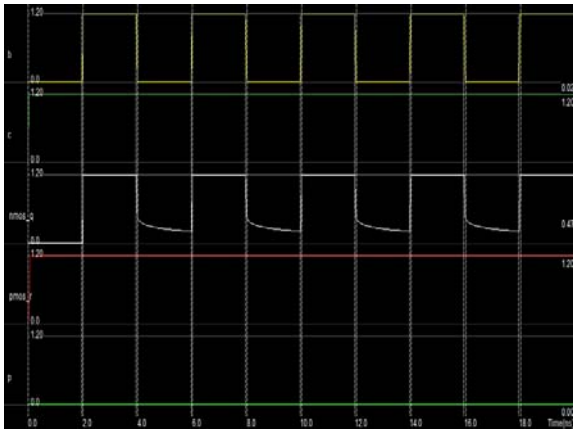


Fig 5(b) : Block diagram of the Proposed 3-to-8 RFD

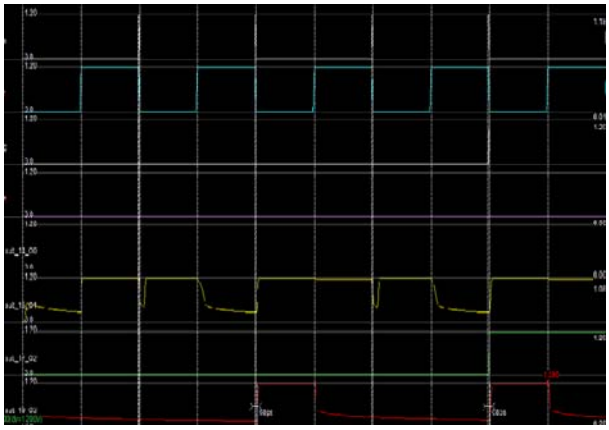
SIMULATION RESULTS



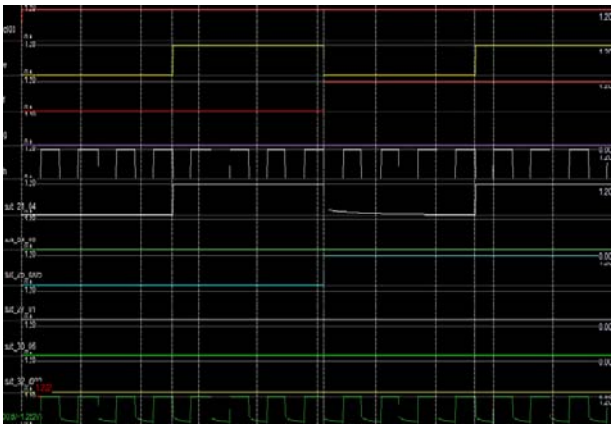
Timing diagram of Feynamn double gate



Timing diagram of Fredkin gate



Timing diagram of proposed 2-to-4 RFD



Timing diagram of proposed 3-to-8 RFD

CONCLUSION

In this paper, we presented the design methodologies of an n-to-2^n reversible fault tolerant decoder,where n is the number of data bits. We proposed reversible fault tolerant decoder by using fault tolerant gates with constant inputs and quantum cost.Reversible fault tolerant decoders can be used in parallel circuits, network components and digital signal processing etc..Transistor implementation of the decoder showed that proposed fault tolerant decoder correctly.

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